FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. IMEC65.1CPCP1	APPLICATION NO. 09/273,089
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)	APPLICANT Schaumont et al.	
	FILING DATE March 19, 1999	GROUP ~~2125~~ 2128

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
RF	1	5,623,418	4/22/1997	Rosotker et al.	716	1	
RF	2	5,933,356	8/1999	Rostoker et al.	703	~~16~~	
RF	3	6,324,678	11/2001	Damgelo et al.	716	18	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	4	0 445 942 A2	2/25/1991	EP	—	—		

EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
RF	5	Altmeyer, et al. "Generating ECAD Framework Code from Abstract Models," Proc. of the 32nd ACM/IEEE Conf. on Design Automation, 1995, pp. 88-93.
RF	6	Basu, et al. "DOORS: An Object-Oriented CAD System for High Level Synthesis," IEE Proceedings - Computers and Digital Techniques, 1997, Vol. 144, Issue 5, pp. 331-342.
RF	7	Bill Lin. "System Design Tools for Broadband Telecom Network Applications" XP-002114729, 1996, pp. 23-26.
RF	8	Bolsens, et al. "Hardware/Software Co-Design of Digital Telecommunications Systems," Proceedings of the IEEE, 1997, Vol. 85, Issue 3, pp. 391-418.
RF	9	Bredenfeld et al. "Tool Integration and Construction using General Graph-based Design Representations," Proc. of the 32nd ACM/IEEE Conf. on Design Automation, 1995.
RF	10	Burr, et al. "OPERAS in a DSP CAD Environment," Proceedings of the European Design Automation Conference, 1994, pp. 130-135.
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EXAMINER	Russell Fred	DATE CONSIDERED	5/3/04

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	FILING DATE March 19, 1999	GROUP ~~2123~~ 2128

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RF	18	Pangrle, et al. "An Integrated Multi-level Synthesis System," First International Workshop on Rapid System Prototyping, 1990, pp. 167-175.
RF	19	Sarkar, et al. "Synchronization of Communicating Modules and Processes in High Level Synthesis," Proceedings of the 8th International Conference on VLSI Design, 1995, pp. 87-92.
RF	20	Schaumont, et al. "Synthesis of Multi-rate and Variable Rate Circuits for High Speed Telecommunications Applications" XP-002114732, 1997, pp. 542-546.
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RF	26	Yang, et al. L.; Perkowski, M.A.; Smith, D.; "Object-Oriented Design of an Expandable Hardware Description Language Analyzer for a High Level Synthesis System," Proceedings of the Twenty-fifth Hawaii International Conference on System Sciences, 1992, Vol. 2. pp.
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EXAMINER Russell Fred	DATE CONSIDERED 5/3/04

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